Asynchronous Circuit Design. Chris J. Myers

ISBNs: 0-471-41543-X (Hardback); 0-471-22414-6 (Electronic)

References

1. M. Abadi and L. Lamport. An old-fashioned recipe for real time, 1993.
2. M. Afghahi and C. Svensson. Performance of synchronous and asynchronous schemes for VLSI systems. *IEEE Transactions on Computers*, 41(7):858–872, July 1992.
3. V. Akella. *An Integrated Framework for the Automatic Synthesis of Efficient Self-Timed Circuits from Behavioral Specifications.* PhD thesis, University of Utah, 1992.
4. V. Akella and G. Gopalakrishnan. SHILPA: A high-level synthesis system for self-timed circuits. In *Proc. International Conference on Computer-Aided Design (ICCAD)*, pages 587–591. IEEE Computer Society Press, Los Alamitos, CA, November 1992.
5. V. Akella and G. Gopalakrishnan. Specification and validation of control-intensive IC's in hopCP. *IEEE Transactions on Software Engineering*, 20(6):405–423, 1994.
6. V. Akella, N. H. Vaidya, and G. R. Redinbo. Asynchronous comparison-based decoders for delay-insensitive codes. *IEEE Transactions on Computers*, 47(7):802–811, July 1998.
7. R. Alur. *Techniques for Automatic Verification of Real-Time Systems.* PhD thesis, Stanford University, August 1991.
8. R. Alur and D. L. Dill. A theory of timed automata. *Theoretical Computer Science*, 126:183–235, 1994.
9. R. Alur and R. P. Kurshan. Timing analysis in cospan. In *Hybrid Systems III.* Springer-Verlag, New York, 1996.

10. S. S. Appleton, S. V. Morton, and M. J. Liebelt. The design of a fast asynchronous microprocessor. *IEEE Technical Committee on Computer Architecture Newsletter*, October 1995.

11. D. B. Armstrong, A. D. Friedman, and P. R. Menon. Realization of asynchronous sequential circuits without inserted delay elements. *IEEE Transactions on Computers*, C-17(2):129–134, February 1968.

12. D. B. Armstrong, A. D. Friedman, and P. R. Menon. Design of asynchronous circuits assuming unbounded gate delays. *IEEE Transactions on Computers*, C-18(12):1110–1120, December 1969.

13. F. Asai, S. Komori, and T. Tamura. Self-timed design for a data-driven microprocessor. *IEICE Transactions*, E 74(11):3757–3765, November 1991.

14. *Proc. 6th International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC 2000)*, Eilat, Israel, April 2000. IEEE Computer Society Press, Los Alamitos, CA.

15. *Proc. 7th International Symposium on Asynchronous Circuits and Systems (ASYNC 2001)*, Salt Lake City, UT, March 2001. IEEE Computer Society Press, Los Alamitos, CA.

16. *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC'94)*, Salt Lake City, UT, November 1994. IEEE Computer Society Press, Los Alamitos, CA.

17. *Proc. 2nd International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC'96)*, Aizu-Wakamatsu, Fukushima, Japan, March 1996. IEEE Computer Society Press, Los Alamitos, CA.

18. *Proc. 3rd International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC'97)*, Eindhoven, The Netherlands, April 1997. IEEE Computer Society Press, Los Alamitos, CA.

19. *Proc. 4th International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC'98)*, San Diego, CA, April 1998. IEEE Computer Society Press, Los Alamitos, CA.

20. *Proc. 5th International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC'99)*, Barcelona, Spain, April 1999. IEEE Computer Society Press, Los Alamitos, CA.

21. A. Bailey, G. A. McCaskill, and G. J. Milne. An exercise in the automatic verification of asynchronous designs. *Formal Methods in System Design*, 4:213–242, 1994.

22. T. S. Balraj and M. J. Foster. Miss Manners: A specialized silicon compiler for synchronizers. In Charles E. Leierson, editor, *Advanced Research in VLSI*, pages 3–20. MIT Press, Cambridge, MA, April 1986.

23. J. C. Barros and B. W. Johnson. Equivalence of the arbiter, the synchronizer, the latch, and the inertial delay. *IEEE Transactions on Computers*, 32(7):603–614, July 1983.

24. W. S. Bartky. A theory of asynchronous circuits III. Technical Report 96, University of Illinois, Urbana, IL, 1960.

25. P. Beerel and T. H.-Y. Meng. Automatic gate-level synthesis of speed-independent circuits. In *Proc. International Conference on Computer-Aided Design (ICCAD)*, pages 581–587. IEEE Computer Society Press, Los Alamitos, CA, November 1992.

26. P. A. Beerel, J. R. Burch, and T. H.-Y. Meng. Checking combinational equivalence of speed-independent circuits. *Formal Methods in System Design*, March 1998.

27. P. A. Beerel and T. H.-Y. Meng. Semi-modularity and testability of speed-independent circuits. *Integration, the VLSI Journal*, 13(3):301–322, September 1992.

28. P. A. Beerel, T. H.-Y. Meng, and J. Burch. Efficient verification of determinate speed-independent circuits. In *Proc. International Conference on Computer-Aided Design (ICCAD)*, pages 261–267. IEEE Computer Society Press, Los Alamitos, CA, November 1993.

29. P. A. Beerel, C. J. Myers, and T. H.-Y. Meng. Covering conditions and algorithms for the synthesis of speed-independent circuits. *IEEE Transactions on Computer-Aided Design*, March 1998.

30. J. Beister. A unified approach to combinational hazards. *IEEE Transactions on Computers*, C-23(6), 1974.

31. W. Belluomini. *Algorithms for the Synthesis and Verification of Timed Circuits and Systems.* PhD thesis, University of Utah, 1999.

32. W. Belluomini and C. J. Myers. Verification of timed systems using posets. In *Proc. International Conference on Computer Aided Verification.* Springer-Verlag, New York, 1998.

33. W. Belluomini and C. J. Myers. Timed state space exploration using posets. *IEEE Transactions on Computer-Aided Design*, 19(5):501–520, May 2000.

34. W. Belluomini and C. J. Myers. Timed circuit verification using tel structures. *IEEE Transactions on Computer-Aided Design*, 20(1):129–146, January 2001.

35. C. H. van Berkel and C. E. Molnar. Beware the three-way arbiter. *IEEE Journal of Solid-State Circuits*, 34(6):840–848, June 1999.

36. K. v. Berkel. *Handshake Circuits: An Intermediary Between Communicating Processes and VLSI.* PhD thesis, Eindhoven University of Technology, 1992.

37. K. v. Berkel. *Handshake Circuits: An Asynchronous Architecture for VLSI Programming*, volume 5 of *International Series on Parallel Computation.* Cambridge University Press, New York, 1993.

38. K. v. Berkel, R. Burgess, J. Kessels, A. Peeters, M. Roncken, and F. Schalij. A fully-asynchronous low-power error corrector for the DCC player. *IEEE Journal of Solid-State Circuits*, 29(12):1429–1439, December 1994.

39. K. v. Berkel, J. Kessels, M. Roncken, R. Saeijs, and F. Schalij. The VLSI-programming language Tangram and its translation into handshake circuits. In *Proc. European Conference on Design Automation (EDAC)*, pages 384–389, 1991.

40. K. v. Berkel and M. Rem. VLSI programming of asynchronous circuits for low power. In G. Birtwistle and A. Davis, editors, *Asynchronous Digital Circuit*

Design, Workshops in Computing, pages 152–210. Springer-Verlag, New York, 1995.

41. C. Berthet and E. Cerny. An algebraic model for asynchronous circuits verification. *IEEE Transactions on Computers*, 37(7):835–847, July 1988.

42. A. Blake. *Canonical Expressions in Boolean Algebra.* PhD thesis, University of Chicago, 1937.

43. M. Blaum and J. Bruck. Coding for skew-tolerant parallel asynchronous communications. *IEEE Transactions on Information Theory*, 39(2):379–388, March 1993.

44. M. Blaum and J. Bruck. Delay-insensitive pipelined communication on parallel buses. *IEEE Transactions on Computers*, 44(5):660–668, May 1995.

45. M. Bozga, O. Maler, A. Pnueli, and S. Yovine. Some progress in the symbolic verification of timed automata. In *Proc. International Conference on Computer Aided Verification*, 1997.

46. H. C. Brearley. ILLIAC II: A short description and annotated bibliography. *IEEE Transactions on Computers*, 14(6):399–403, June 1965.

47. J. G. Bredeson. Synthesis of multiple-input change hazard-free combinational switching circuits without feedback. *International Journal of Electronics (GB)*, 39(6):615–624, December 1975.

48. J. G. Bredeson and P. T. Hulina. Elimination of static and dynamic hazards for multiple input changes in combinational switching circuits. *Information and Control*, 20:114–224, 1972.

49. F. Brown. *Boolean Reasoning: The Logic of Boolean Equations.* Kluwer Academic Publishers, Boston, 1990.

50. M. C. Browne, E. M. Clarke, D. L. Dill, and B. Mishra. Automatic verification of sequential circuits using temporal logic. *IEEE Transactions on Computers*, 35(12):1035–1044, December 1986.

51. J. Bruno and S. M. Altman. A theory of asynchronous control networks. *IEEE Transactions on Computers*, 20(6):629–638, June 1971.

52. E. Brunvand. *Translating Concurrent Communicating Programs into Asynchronous Circuits.* PhD thesis, Carnegie Mellon University, 1991.

53. E. Brunvand. Designing self-timed systems using concurrent programs. *Journal of VLSI Signal Processing*, 7(1/2):47–59, February 1994.

54. J. A. Brzozowski and J. C. Ebergen. On the delay-sensitivity of gate networks. *IEEE Transactions on Computers*, 41(11):1349–1360, November 1992.

55. J. A. Brzozowski and C.-J. Seger. A characterization of ternary simulation of gate networks. *IEEE Transactions on Computers*, C-36(11):1318–1327, November 1987.

56. J. A. Brzozowski and C.-J. Seger. A unified framework for race analysis of asynchronous networks. *Journal of the ACM*, 36(1):20–45, January 1989.

57. J. A. Brzozowski and C.-J. H. Seger. *Asynchronous Circuits.* Springer-Verlag, New York, 1995.

58. J. A. Brzozowski and S. Singh. Definite asynchronous sequential circuits. *IEEE Transactions on Computers*, C-17(1):18–26, January 1968.

59. J. A. Brzozowski and M. Yoeli. Practical approach to asynchronous gate networks. *Proceedings of the IEE*, 123(6):495–498, June 1976.

60. J. A. Brzozowski and M. Yoeli. On a ternary model of gate networks. *IEEE Transactions on Computers*, C-28(3):178–184, March 1979.

61. J. R. Burch. Combining ctl, trace theory and timing models. In *Proc. First Workshop on Automatic Verification Methods for Finite State Systems*, 1989.

62. J. R. Burch. Modeling timing assumptions with trace theory. In *Proc. International Conference on Computer Design (ICCD)*, 1989.

63. J. R. Burch. *Trace Algebra for Automatic Verification of Real-Time Concurrent Systems*. PhD thesis, Carnegie Mellon University, 1992.

64. S. M. Burns. Automated compilation of concurrent programs into self-timed circuits. Master's thesis, California Institute of Technology, 1988.

65. S. M. Burns. *Performance Analysis and Optimization of Asynchronous Circuits*. PhD thesis, California Institute of Technology, 1991.

66. S. M. Burns. General condition for the decomposition of state holding elements. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*. IEEE Computer Society Press, Los Alamitos, CA, March 1996.

67. S. M. Burns and A. J. Martin. Syntax-directed translation of concurrent programs into self-timed circuits. In J. Allen and F. T. Leighton, editors, *Advanced Research in VLSI*, pages 35–50. MIT Press, Cambridge, MA, 1988.

68. S. M. Burns and A. J. Martin. Synthesis of self-timed circuits by program transformation. In G. J. Milne, editor, *The Fusion of Hardware Design and Verification*, pages 99–116. Elsevier Science Publishers, New York, 1988.

69. J. Calvo, J. I. Acha, and M. Valencia. Asynchronous modular arbiter. *IEEE Transactions on Computers*, 35(1):67–70, January 1986.

70. I. Catt. Time loss through gating of asynchronous logic signal pulses. *IEEE Transactions on Electronic Computers*, EC-15:108–111, February 1966.

71. S. Chakraborty. *Polynomial-Time Techniques for Approximate Timing Analysis of Asynchronous Systems*. PhD thesis, Stanford University, August 1998.

72. S. Chakraborty, D. L. Dill, and K. Y. Yun. Min-max timing analysis and an application to asynchronous circuits. *Proceedings of the IEEE*, 87(2):332–346, February 1999.

73. S. T. Chakradhar, S. Banerjee, R. K. Roy, and D. K. Pradhan. Synthesis of initializable asynchronous circuits. *IEEE Transactions on VLSI Systems*, 4(2):254–263, June 1996.

74. V. Chandramouli, E. Brunvand, and K. F. Smith. Self-timed design in GaAs: Case study of a high-speed, parallel multiplier. *IEEE Transactions on VLSI Systems*, 4(1):146–149, March 1996.

75. T. J. Chaney and C. E. Molnar. Anomalous behavior of synchronizer and arbiter circuits. *IEEE Transactions on Computers*, C-22(4):421–422, April 1973.

76. C.-M. Chang and S.-L. Lu. Design of a static MIMD data flow processor using micropipelines. *IEEE Transactions on VLSI Systems*, 3(3):370–378, September 1995.

77. D. M. Chapiro. *Globally-Asynchronous Locally-Synchronous Systems.* PhD thesis, Stanford University, October 1984.

78. J. F. Chappel and S. G. Zaky. EMI effects and timing design for increased reliability in digital systems. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 44(2):130–142, February 1997.

79. T. I. Chappell, B. A. Chappell, S. E. Schuster, J. W. Allan, S. P. Klepner, R. V. Joshi, and R. L. Franch. A 2-ns cycle, 3.8-ns access 512-kb CMOS ECL SRAM with a fully pipelined architecture. *IEEE Journal of Solid-State Circuits*, 26(11):1577–1585, November 1991.

80. F.-C. Cheng, S. H. Unger, and M. Theobald. Self-timed carry-lookahead adders. *IEEE Transactions on Computers*, 49(7):659–672, July 2000.

81. W.-C. Chou, P. A. Beerel, and K. Y. Yun. Average-case technology mapping of asynchronous burst-mode circuits. *IEEE Transactions on Computer-Aided Design*, 18(10):1418–1434, October 1999.

82. T.-A. Chu. On the models for designing VLSI asynchronous digital circuits. *Integration, the VLSI Journal*, 4(2):99–113, June 1986.

83. T.-A. Chu. *Synthesis of Self-Timed VLSI Circuits from Graph-Theoretic Specifications.* PhD thesis, MIT Laboratory for Computer Science, June 1987.

84. T.-A. Chu. Synthesis of hazard-free control circuits from asynchronous finite state machine specifications. *Journal of VLSI Signal Processing*, 7(1/2):61–84, February 1994.

85. H. Y. H. Chuang and S. Das. Synthesis of multiple-input change asynchronous machines using controlled excitation and flip-flops. *IEEE Transactions on Computers*, C-22(12):1103–1109, December 1973.

86. Y. H. Chuang. Transition logic circuits and a synthesis method. *IEEE Transactions on Computers*, C-18(2):154–168, February 1969.

87. W. A. Clark. Macromodular computer systems. In *AFIPS Conference Proc.: 1967 Spring Joint Computer Conference*, volume 30, pages 335–336. Academic Press, New York, 1967.

88. W. A. Clark and C. E. Molnar. Macromodular computer systems. In R. W. Stacy and B. D. Waxman, editors, *Computers in Biomedical Research*, volume IV, chapter 3, pages 45–85. Academic Press, New York, 1974.

89. B. Coates, A. Davis, and K. Stevens. The Post Office experience: Designing a large asynchronous chip. *Integration, the VLSI Journal*, 15(3):341–366, October 1993.

90. P. Corsini. Self-synchronizing asynchronous arbiter. *Digital Processes*, 1:67–73, 1975.

91. P. Corsini. Speed-independent asynchronous arbiter. *IEE Journal on Computers and Digital Techniques*, 2(5):221–222, October 1979.

92. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, E. Pastor, and A. Yakovlev. Decomposition and technology mapping of speed-independent

circuits using Boolean relations. *IEEE Transactions on Computer-Aided Design*, 18(9), September 1999.

93. J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. A region-based theory for state assignment in speed-independent circuits. *IEEE Transactions on Computer-Aided Design*, 16(8):793–812, August 1997.
94. O. Coudert and J. C. Madre. New ideas for solving covering problems. In *Proc. ACM/IEEE Design Automation Conference*, pages 641–646, June 1995.
95. G. R. Couranz and D. F. Wann. Theoretical and experimental behavior of synchronizers operating in the metastable region. *IEEE Transactions on Computers*, 24(6):604–616, June 1975.
96. I. David, R. Ginosar, and M. Yoeli. An efficient implementation of boolean functions as self-timed circuits. *IEEE Transactions on Computers*, 41(1):2–11, January 1992.
97. I. David, R. Ginosar, and M. Yoeli. Implementing sequential machines as self-timed circuits. *IEEE Transactions on Computers*, 41(1):12–17, January 1992.
98. R. David. Modular design of asynchronous circuits defined by graphs. *IEEE Transactions on Computers*, 26(8):727–737, August 1977.
99. A. Davis. Synthesizing asynchronous circuits: Practice and experience. In G. Birtwistle and A. Davis, editors, *Asynchronous Digital Circuit Design*, Workshops in Computing, pages 104–150. Springer-Verlag, New York, 1995.
100. A. Davis, B. Coates, and K. Stevens. Automatic synthesis of fast compact asynchronous control circuits. In S. Furber and M. Edwards, editors, *Asynchronous Design Methodologies*, volume A-28 of *IFIP Transactions*, pages 193–207. Elsevier Science Publishers, New York, 1993.
101. A. Davis, B. Coates, and K. Stevens. The Post Office experience: Designing a large asynchronous chip. In *Proc. Hawaii International Conference on System Sciences*, volume I, pages 409–418. IEEE Computer Society Press, Los Alamitos, CA, January 1993.
102. A. L. Davis. The architecture and system method of ddm-1: A recursive-structured data driven machine. In *Proc. 5th Annual Symposium on Computer Architecture*, 1978.
103. A. L. Davis. A data-driven machine architecture suitable for VLSI implementation. In C. L. Seitz, editor, *Proc. Caltech Conference on Very Large Scale Integration*, pages 479–494, January 1979.
104. P. Day and J. V. Woods. Investigation into micropipeline latch design styles. *IEEE Transactions on VLSI Systems*, 3(2):264–272, June 1995.
105. M. Dean, T. Williams, and D. Dill. Efficient self-timing with level-encoded 2-phase dual-rail (LEDR). In C. H. Séquin, editor, *Advanced Research in VLSI*, pages 55–70. MIT Press, Cambridge, MA, 1991.
106. M. E. Dean. *STRiP: A Self-Timed RISC Processor Architecture*. PhD thesis, Stanford University, 1992.
107. M. E. Dean, D. L. Dill, and M. Horowitz. Self-timed logic using current-sensing completion detection (CSCD). *Journal of VLSI Signal Processing*, 7(1/2):7–16, February 1994.

108. Z. J. Deng, N. Yoshikawa, S. R. Whiteley, and T. Van Duzer. Data-driven self-timed RSFQ digital integrated circuit and system. *IEEE Transactions on Applied Superconductivity*, 7(2):3634–3637, June 1997.

109. Z. J. Deng, N. Yoshikawa, S. R. Whiteley, and T. Van Duzer. Data-driven self-timed RSFQ high-speed test system. *IEEE Transactions on Applied Superconductivity*, 7(4):3830–3833, December 1997.

110. Z. J. Deng, N. Yoshikawa, S. R. Whiteley, and T. Van Duzer. Self-timing and vector processing in RSFQ digital circuit technology. *IEEE Transactions on Applied Superconductivity*, 9(1):7–17, March 1999.

111. Z. J. Deng, N. Yoshikawa, S. R. Whiteley, and T. Van Duzer. Simulation and 18 Gb/s testing of a data-driven self-timed RSFQ demultiplexer. *IEEE Transactions on Applied Superconductivity*, 9(2):4349–4352, June 1999.

112. S. Devadas, K. Keutzer, S. Malik, and A. Wang. Verification of asynchronous interface circuits with bounded wire delays. *Journal of VLSI Signal Processing*, 7(1/2):161–182, February 1994.

113. D. L. Dill. Trace theory for automatic hierarchical verification of speed-independent circuits. In J. Allen and F. T. Leighton, editors, *Advanced Research in VLSI*, pages 51–65. MIT Press, Cambridge, MA, 1988.

114. D. L. Dill. Timing assumptions and verification of finite-state concurrent systems. In *Proc. Workshop on Automatic Verification Methods for Finite-State Systems*, 1989.

115. D. L. Dill. *Trace Theory for Automatic Hierarchical Verification of Speed-Independent Circuits.* ACM Distinguished Dissertations. MIT Press, Cambridge, MA, 1989.

116. D. L. Dill and E. M. Clarke. Automatic verification of asynchronous circuits using temporal logic. *IEE Proceedings, Computers and Digital Techniques*, 133:272–282, September 1986.

117. J. Ebergen and R. Berks. VERDECT: A verifier for asynchronous circuits. *IEEE Technical Committee on Computer Architecture Newsletter*, October 1995.

118. J. Ebergen and R. Berks. Response time properties of linear asynchronous pipelines. *Proceedings of the IEEE*, 87(2):308–318, February 1999.

119. J. C. Ebergen. *Translating Programs into Delay-Insensitive Circuits.* PhD thesis, Eindhoven University of Technology, 1987.

120. J. C. Ebergen. *Translating Programs into Delay-Insensitive Circuits*, volume 56 of *CWI Tract.* Centre for Mathematics and Computer Science, 1989.

121. J. C. Ebergen. A formal approach to designing delay-insensitive circuits. *Distributed Computing*, 5(3):107–119, 1991.

122. E. B. Eichelberger. Hazard detection in combinational and sequential switching circuits. *IBM Journal of Research and Development*, 9:90–99, March 1965.

123. E. A. Emerson. Temporal and modal logic. In J. v. Leeuwen, editor, *Handbook of Theoretical Computer Science*, pages 995–1072. North-Holland, Amsterdam, 1989.

124. P. D. Fisher and S.-F. Wu. Race-free state assignments for synthesizing large-scale asynchronous sequential logic circuits. *IEEE Transactions on Computers*, 42(9):1025–1034, September 1993.

125. W. Fleischhammer and O. Dortok. The anomalous behavior of flip-flops in synchronizer circuits. *IEEE Transactions on Computers*, 28(3):273–276, March 1979.

126. J. Frackowiak. Methoden der analyse und synthese von hasardarmen schaltnetzen mit minimalen kosten i. *Elektronische Informationsverarbeitung und Kybernetik*, 10(2/3):149–187, 1974.

127. E. H. Frank and R. F. Sproull. A self-timed static RAM. In R. Bryant, editor, *Proc. 3rd Caltech Conference on VLSI*, pages 275–285. Computer Science Press, Rockville, MD, 1983.

128. A. D. Friedman, R. L. Graham, and J. D. Ullman. Universal single transition time asynchronous state assignments. *IEEE Transactions on Computers*, C-18:541–547, June 1969.

129. A. D. Friedman and P. R. Menon. Synthesis of asynchronous sequential circuits with multiple-input changes. *IEEE Transactions on Computers*, C-17(6):559–566, June 1968.

130. A. D. Friedman and P. R. Menon. Systems of asynchronously operating modules. *IEEE Transactions on Computers*, 20:100–104, 1971.

131. R. M. Fuhrer, B. Lin, and S. M. Nowick. Symbolic hazard-free minimization and encoding of asynchronous finite state machines. In *Proc. International Conference on Computer-Aided Design (ICCAD)*. IEEE Computer Society Press, Los Alamitos, CA, 1995.

132. R. M. Fuhrer and S. M. Nowick. OPTIMISTA: State minimization of asynchronous FSMs for optimum output logic. In *Proc. International Conference on Computer-Aided Design (ICCAD)*, pages 7–13. IEEE Computer Society Press, Los Alamitos, CA, November 1999.

133. S. B. Furber and P. Day. Four-phase micropipeline latch control circuits. *IEEE Transactions on VLSI Systems*, 4(2):247–253, June 1996.

134. S. B. Furber, J. D. Garside, and D. A. Gilbert. AMULET3: A high-performance self-timed ARM microprocessor. In *Proc. International Conference on Computer Design (ICCD)*, October 1998.

135. S. B. Furber, J. D. Garside, P. Riocreux, S. Temple, P. Day, J. Liu, and N. C. Paver. AMULET2e: An asynchronous embedded controller. *Proceedings of the IEEE*, 87(2):243–256, February 1999.

136. H. v. Gageldonk, D. Baumann, K. v. Berkel, D. Gloor, A. Peeters, and G. Stegmann. An asynchronous low-power 80c51 microcontroller. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 96 107, 1998.

137. M. J. Gamble. A novel current-sensing completion-detection circuit adapted to the micropipeline methodology. Master's thesis, University of Manitoba, Canada, 1994.

138. J. D. Garside, S. B. Furber, and S.-H. Chung. AMULET3 revealed. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 51–59, April 1999.

139. B. Gilchrist, J. H. Pomerene, and S. Y. Wong. Fast carry logic for digital computers. *IRE Transactions on Electronic Computers*, EC-4(4):133–136, December 1955.

140. J. Gimpel. A reduction technique for prime implicant tables. *IEEE Transactions on Electronic Computers*, EC-14:535–541, August 1965.

141. R. Ginosar, R. Kol, K. Stevens, P. Beerel, K. Yun, C. Myers, and S. Rotem. Apparatus and method for parallel processing and self-timed serial marking of variable length instructions. U.S. patent 5,978,899 granted November 2, 1999.

142. R. Ginosar, R. Kol, K. Stevens, P. Beerel, K. Yun, C. Myers, and S. Rotem. Apparatus and method for self-timed marking of variable length instructions having length-affecting prefix bytes. U.S. patent 5,948,096 granted September 7, 1999.

143. R. Ginosar, R. Kol, K. Stevens, P. Beerel, K. Yun, C. Myers, and S. Rotem. Branch instruction handling in a self-timed marking system. U.S. patent 5,931,944 granted August 3, 1999.

144. R. Ginosar, R. Kol, K. Stevens, P. Beerel, K. Yun, C. Myers, and S. Rotem. Efficient self-timed marking of lengthy variable length instructions. U.S. patent 5,941,982 granted August 24, 1999.

145. S. Ginsburg. On the reduction of superfluous states in sequential machines. *Journal of the ACM*, 6:252 282, April 1959.

146. S. Ginsburg. A synthesis technique for minimal state sequential machines. *IRE Transactions on Electronic Computers*, EC-8:13–24, March 1959.

147. A. De Gloria and M. Olivieri. Efficient semicustom micropipeline design. *IEEE Transactions on VLSI Systems*, 3(3):464–469, September 1995.

148. A. De Gloria and M. Olivieri. Statistical carry lookahead adders. *IEEE Transactions on Computers*, 45(3):340–347, March 1996.

149. P. Godefroid. Using partial orders to improve automatic verification methods. In *Proc. International Workshop on Computer Aided Verification*, pages 176–185, June 1990.

150. G. Gopalakrishnan and V. Akella. High level optimizations in compiling process descriptions to asynchronous circuits. *Journal of VLSI Signal Processing*, 7(1/2):33–45, February 1994.

151. G. Gopalakrishnan, E. Brunvand, N. Michell, and S. Nowick. A correctness criterion for asynchronous circuit validation and optimization. *IEEE Transactions on Computer-Aided Design*, 13(11):1309–1318, November 1994.

152. G. Gopalakrishnan, P. Kudva, and E. Brunvand. Peephole optimization of asynchronous macromodule networks. *IEEE Transactions on VLSI Systems*, 7(1):30–37, March 1999.

153. E. Grass, V. Bartlett, and I. Kale. Completion-detection techniques for asynchronous circuits. *IEICE Transactions on Information and Systems*, E80-D(3):344–350, March 1997.

154. E. Grass and S. Jones. Activity monitoring completion detection (AMCD): A new approach to achieve self-timing. *Electronics Letters*, 32(2):86–88, 1996.

155. A. Grasselli and F. Luccio. A method for minimizing the number of internal states in incompletely specified sequential networks. *IEEE Transactions on Electronic Computers*, pages 350–359, June 1965.

156. A. Grasselli and F. Luccio. Some covering problems in switching theory. In G. Biorci, editor, *Network and Switching Theory*. Academic Press, 1966.

157. J. Gu and R. Puri. Asynchronous circuit synthesis with boolean satisfiability. *IEEE Transactions on Computer-Aided Design*, 14(8):961–973, August 1995.

158. G. D. Hachtel and F. Somenzi. *Logic Synthesis and Verification Algorithms*. Kluwer Academic Publishers, Boston, 1996.

159. K. Hamaguchi, H. Hiraishi, and S. Yajima. Formal verification of speed-dependent asynchronous circuits using symbolic model checking of branching time regular temporal logic. In K. G. Larsen and A. Skou, editors, *Proc. International Workshop on Computer Aided Verification*, volume 575 of *Lecture Notes in Computer Science*, pages 410–420. Springer-Verlag, New York, 1991.

160. A. B. Hayes. Stored state asynchronous sequential circuits. *IEEE Transactions on Computers*, C-30(8):596–600, August 1981.

161. A. B. Hayes. Self-timed IC design with PPL's. In R. Bryant, editor, *Proc. 3rd Caltech Conference on VLSI*, pages 257–274. Computer Science Press, Rockville, MD, 1983.

162. P. J. Hazewindus. *Testing Delay-Insensitive Circuits*. PhD thesis, California Institute of Technology, 1992.

163. A. Hemani, T. Meincke, S. Kumar, A. Postula, T. Olsson, P. Nilsson, J. Öberg, P. Ellervee, and D. Lundqvist. Lowering power consumption in clock by using globally asynchronous, locally synchronous design style. In *Proc. ACM/IEEE Design Automation Conference*, 1999.

164. J. Hennessy and D. Patterson. *Computer Organization & Design: The Hardware/Software Interface*. Morgan Kaufmann, San Francisco, 1998.

165. Masaharu Hirayama. A silicon compiler system based on asynchronous architecture. *IEEE Transactions on Computer-Aided Design*, 6(3):297–304, May 1987.

166. C. A. R. Hoare. Communicating sequential processes. *Communications of the ACM*, 21(8):666–677, August 1978.

167. C. A. R. Hoare. *Communicating Sequential Processes*. Prentice-Hall, Englewood Cliffs, NJ, 1985.

168. L. A. Hollaar. Direct implementation of asynchronous control units. *IEEE Transactions on Computers*, C-31(12):1133–1141, December 1982.

169. J. U. Horstmann, H. W. Eichel, and R. L. Coates. Metastability behavior of CMOS ASIC flip-flops in theory and test. *IEEE Journal of Solid-State Circuits*, 24(1):146–157, February 1989.

170. D. A. Huffman. The synthesis of sequential switching circuits. *Journal of the Franklin Institute*, March/April 1954.

171. D. A. Huffman. Design of hazard-free switching circuits. *Journal of the ACM*, 4:47–62, January 1957.

172. D. A. Huffman. The synthesis of sequential switching circuits. In E. F. Moore, editor, *Sequential Machines: Selected Papers*. Addison-Wesley, Reading, MA, 1964.

173. H. Hulgaard. *Timing Analysis and Verification of Timed Asynchronous Circuits*. PhD thesis, University of Washington, 1995.

174. H. Hulgaard and S. M. Burns. Bounded delay timing analysis of a class of CSP programs. *Formal Methods in System Design*, 11(3):265–294, October 1997.

175. H. Hulgaard, S. M. Burns, T. Amon, and G. Borriello. An algorithm for exact bounds on the time separation of events in concurrent systems. *IEEE Transactions on Computers*, 44(11):1306–1317, November 1995.

176. H. Hulgaard, S. M. Burns, and G. Borriello. Testing asynchronous circuits: A survey. *Integration, the VLSI Journal*, 19(3):111–131, November 1995.

177. M. Hurtado. *Structure and Performance of Asymptotically Bistable Dynamical Systems*. PhD thesis, Sever Institute of Technology, Washington University, 1975.

178. W. Hwang, R. V. Joshi, and G. D. Gristede. A scannable pulse-to-static conversion register array for self-timed circuits. *IEEE Journal of Solid-State Circuits*, 35(1):125–128, January 2000.

179. S. Robinson III and R. House. Gimpel's reduction technique extended to the covering problem with costs. *IEEE Transactions on Electronic Computers*, EC-16:509–514, February 1967.

180. H. Jacobson, C. J. Myers, and G. Gopalakrishnan. Achieving fast and exact hazard-free logic minimization of extended burst-mode gC finite state machines. In *Proc. International Conference on Computer-Aided Design (ICCAD)*, November 2000.

181. K. W. James and K. Y. Yun. Average-case optimized transistor-level technology mapping of extended burst-mode circuits. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 70–79, 1998.

182. D. Johnson, V. Akella, and B. Stott. Micropipelined asynchronous discrete cosine transform (DCT/IDCT) processor. *IEEE Transactions on VLSI Systems*, 6(4):731–740, December 1998.

183. M. B. Josephs and J. T. Yantchev. CMOS design of the tree arbiter element. *IEEE Transactions on VLSI Systems*, 4(4):472–476, December 1996.

184. J. R. Jump and P. S. Thiagarajan. On the interconnection of asynchronous control structures. *Journal of the ACM*, 22:596–612, October 1975.

185. S. T. Jung and C. S. Jhon. Direct synthesis of efficient speed-independent circuits from deterministic signal transition graphs. In *Proc. International Symposium on Circuits and Systems*, pages 307–310, June 1994.

186. S. T. Jung and C. J. Myers. Direct synthesis of timed asynchronous circuits. In *Proc. International Conference on Computer-Aided Design (ICCAD)*, pages 332–337, November 1999.

187. S. T. Jung, U. S. Park, J. S. Kim, and C. S. Jhon. Automatic synthesis of gate-level speed-independent control circuits from signal transition graphs. In *Proc. International Symposium on Circuits and Systems*, pages 1411–1414, 1995.

188. J.-W. Kang, C.-L. Wey, and P. D. Fisher. Application of bipartite graphs for achieving race-free state assignments. *IEEE Transactions on Computers*, 44(8):1002–1011, August 1995.

189. V. Kantabutra and A. G. Andreou. A state assignment approach to asynchronous CMOS circuit design. *IEEE Transactions on Computers*, 43(4):460–469, April 1994.

190. R. M. Keller. Towards a theory of universal speed-independent modules. *IEEE Transactions on Computers*, C-23(1):21–33, January 1974.

191. R. Kelly and L. E. M. Brackenbury. Design and modelling of a high performance differential bipolar self-timed microprocessor. *IEE Proceedings, Computers and Digital Techniques*, 144(6):371–380, November 1997.

192. J. Kessels, T. Kramer, G. d. Besten, A. Peeters, and V. Timm. Applying asynchronous circuits in contactless smart cards. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 36–44. IEEE Computer Society Press, Los Alamitos, CA, April 2000.

193. J. Kessels and P. Marston. Designing asynchronous standby circuits for a low-power pager. *Proceedings of the IEEE*, 87(2):257–267, February 1999.

194. K. Keutzer, L. Luciano, and A. Sangiovanni-Vincentelli. Synthesis for testability techniques for asynchronous circuits. *IEEE Transactions on Computer-Aided Design*, 14(12):1569–1577, December 1995.

195. A. Khoche. *Testing Macro-Module Based Self-Timed Circuits*. PhD thesis, University of Utah, 1996.

196. K. Killpack, E. Mercer, and C. J. Myers. A standard-cell self-timed multiplier for energy and area critical synchronous systems. In E. Brunvand and C. Myers, editors, *Advanced Research in VLSI*, pages 188–201. IEEE Computer Society Press, Los Alamitos, CA, March 2001.

197. I. Kimura. Extensions of asynchronous circuits and the delay problem I: Good extensions and the delay problem of the first kind. *Journal of Computer and System Sciences*, 2(3):251–287, October 1968.

198. I. Kimura. Extensions of asynchronous circuits and the delay problem II: Spike-free extensions and the delay problem of the second kind. *Journal of Computer and System Sciences*, 5(2):129–162, April 1971.

199. D. J. Kinniment. An evaluation of asynchronous addition. *IEEE Transactions on VLSI Systems*, 4(1):137–140, March 1996.

200. D. J. Kinniment and J. V. Woods. Synchronization and arbitration circuits in digital systems. *Proceedings of the IEE*, 123(10):961–966, October 1976.

201. M. Kishinevsky, A. Kondratyev, L. Lavagno, A. Saldanha, and A. Taubin. Partial-scan delay fault testing of asynchronous circuits. *IEEE Transactions on Computer-Aided Design*, 17(11):1184–1199, November 1998.

202. M. Kishinevsky, A. Kondratyev, A. Taubin, and V. Varshavsky. Analysis and identification of speed-independent circuits on an event model. *Formal Methods in System Design*, 4(1):33–75, 1994.

203. M. Kishinevsky, A. Kondratyev, A. Taubin, and V. Varshavsky. *Concurrent Hardware: The Theory and Practice of Self-Timed Design.* Series in Parallel Computing. Wiley, New York, 1994.

204. L. Kleeman and A. Cantoni. Can redundancy and masking improve the performance of synchronizers. *IEEE Transactions on Computers*, 35:643–646, July 1986.

205. L. Kleeman and A. Cantoni. On the unavoidability of metastable behavior in digital systems. *IEEE Transactions on Computers*, C-36(1):109–112, January 1987.

206. T. Kobayashi, K. Arimoto, Y. Ikeda, M. Hatanaka, K. Mashiko, M. Yamada, and T. Nakano. A high-speed 46K×4 CMOS DRAM using on-chip self-timing techniques. *IEEE Journal of Solid-State Circuits*, 21(5):655–661, October 1986.

207. S. Komori, H. Takata, T. Tamura, F. Asai, T. Ohno, O. Tomisawa, T. Yamasaki, K. Shima, K. Asada, and H. Terada. An elastic pipeline mechanism by self-timed circuits. *IEEE Journal of Solid-State Circuits*, 23(1):111–117, February 1988.

208. S. Komori, H. Takata, T. Tamura, F. Asai, T. Ohno, O. Tomisawa, T. Yamasaki, K. Shima, H. Nishikawa, and H. Terada. A 40-MFLOPS 32-bit floating-point processor with elastic pipeline scheme. *IEEE Journal of Solid-State Circuits*, 24(5):1341–1347, October 1989.

209. A. Kondratyev, J. Cortadella, M. Kishinevsky, L. Lavagno, and A. Yakovlev. Logic decomposition of speed-independent circuits. *Proceedings of the IEEE*, 87(2):347–362, February 1999.

210. A. Kondratyev, M. Kishinevsky, and A. Yakovlev. Hazard-free implementation of speed-independent circuits. *IEEE Transactions on Computer-Aided Design*, 17(9):749–771, September 1998.

211. C. Krieger. Solving state coding problems in timed asynchronous circuits. Master's thesis, University of Utah, 1999.

212. S. A. Kripke. Semantical analysis of modal logic I: Normal propositional calculi. *Zeitschrift fuer Mathematsche Logik und Grundlagen der Mathcematik*, 9:67–96, 1963.

213. P. Kudva, G. Gopalakrishnan, H. Jacobson, and S. M. Nowick. Synthesis of hazard-free customized CMOS complex-gate networks under multiple-input changes. In *Proc. ACM/IEEE Design Automation Conference*, 1996.

214. J. G. Kuhl and S. M. Reddy. A multicode single transition-time state assignment for asynchronous sequential machines. *IEEE Transactions on Computers*, 27:927–934, October 1978.

215. D.S. Kung. Hazard-non-increasing gate-level optimization algorithms. In *Proc. International Conference on Computer-Aided Design (ICCAD)*, pages 631–634. IEEE Computer Society Press, Los Alamitos, CA, November 1992.

216. I. Kurosawa, H. Nakagawa, M. Aoyagi, M. Maezawa, Y. Kameda, and T. Nanya. A basic circuit for asynchronous superconductive logic using RSFQ gates. *Superconductor-Science-Technology*, 9(4A):A46–49, April 1996.

217. G. Lacroix, P. Marchegay, and G. Piel. Comments on "the anomalous behavior of flip-flops in synchronizer circuits". *IEEE Transactions on Computers*, 31(1):77–78, January 1982.

218. H. Lampinen and O. Vainio. Circuit design for current-sensing completion detection. In *Proc. International Symposium on Circuits and Systems*, volume 2, pages 185–188, June 1998.

219. C. G. Langdon. *Analysis and Synthesis of Asynchronous Circuits Under Different Delay Assumptions.* PhD thesis, Syracuse University, October 1967.

220. C. G. Langdon. Delay-free asynchronous circuits with constrained line delays. *IEEE Transactions on Computers*, 17:1131–1143, December 1968.

221. L. Lavagno. *Synthesis and Testing of Bounded Wire Delay Asynchronous Circuits from Signal Transition Graphs.* PhD thesis, University of California, Berkeley, November 1992.

222. L. Lavagno, K. Keutzer, and A. Sangiovanni-Vincentelli. Synthesis of hazard-free asynchronous circuits with bounded wire delays. *IEEE Transactions on Computer-Aided Design*, 14(1):61–86, January 1995.

223. L. Lavagno, C. W. Moon, R. K. Brayton, and A. Sangiovanni-Vincentelli. An efficient heuristic procedure for solving the state assignment problem for event-based specifications. *IEEE Transactions on Computer-Aided Design*, 14(1):45–60, January 1995.

224. L. Lavagno and A. Sangiovanni-Vincentelli. *Algorithms for Synthesis and Testing of Asynchronous Circuits.* Kluwer Academic Publishers, Boston, 1993.

225. L. Lavagno, N. Shenoy, and A. Sangiovanni-Vincentelli. Linear programming for hazard elimination in asynchronous circuits. *Journal of VLSI Signal Processing*, 7(1/2):137–160, February 1994.

226. Y. Leblebici, H. Özdemir, A. Kepkep, and U. Çilingiroğlu. A compact high-speed (31,5) parallel counter circuit based on capacitive threshold-logic gates. *IEEE Journal of Solid-State Circuits*, 31(8):1177–1183, August 1996.

227. K. Lee and K. Choi. Self-timed divider based on RSD number system. *IEEE Transactions on VLSI Systems*, 4(2):292–295, June 1996.

228. T. W. S. Lee, M. R. Greenstreet, and C.-J. Seger. Automatic verification of asynchronous circuits. *IEEE Design and Test of Computers*, 12(1):24–31, Spring 1995.

229. S. C. Leung and H. F. Li. A syntax-directed translation for the synthesis of delay-insensitive circuits. *IEEE Transactions on VLSI Systems*, 2(2):196–210, June 1994.

230. S. C. Leung and H. F. Li. On the realizability and synthesis of delay-insensitive behaviors. *IEEE Transactions on Computer-Aided Design*, 14(7):833–848, July 1995.

231. L. A. Lev et al. A 64-b microprocessor with multimedia support. *IEEE Journal of Solid-State Circuits*, 30(11):1227–1238, November 1995.

232. M. J. Liebelt and N. Burgess. Detecting exitory stuck-at faults in semimodular asynchronous circuits. *IEEE Transactions on Computers*, 48(4):442–448, April 1999.

233. W. Lim. Design methodology for stoppable clock systems. *IEE Proceedings, Computers and Digital Techniques*, 133(1):65–69, January 1986.

234. B. Lin and S. Devadas. Synthesis of hazard-free multilevel logic under multi-input changes from binary decision diagrams. *IEEE Transactions on Computer-Aided Design*, 14(8):974–985, August 1995.

235. K.-J. Lin, C.-W. Kuo, and C.-S. Lin. Synthesis of hazard-free asynchronous circuits based on characteristic graph. *IEEE Transactions on Computers*, 46(11):1246–1263, November 1997.

236. D. H. Linder and J. C. Harden. Phased logic: Supporting the synchronous design paradigm with delay-insensitive circuitry. *IEEE Transactions on Computers*, 45(9):1031–1044, September 1996.

237. P. F. Lister. Design methodology for self-timed VLSI systems. *IEE Proceedings, Computers and Digital Techniques*, 132(1):25–32, January 1985.

238. C. N. Liu. A state variable assignment method for asynchronous sequential switching circuits. *Journal of the ACM*, 10:209–216, 1963.

239. S. Lubkin. Asynchronous circuits in digital computers. *Mathematical Tables and Other Aids to Computation*, pages 238–241, October 1952.

240. M. Maezawa, I. Kurosawa, M. Aoyagi, H. Nakagawa, Y. Kameda, and T. Nanya. Rapid single-flux-quantum dual-rail logic for asynchronous circuits. *IEEE Transactions on Applied Superconductivity*, 7(2):2705–2708, June 1997.

241. G. Magó. Realization methods for asynchronous sequential circuits. *IEEE Transactions on Computers*, C-20(3):290–297, March 1971.

242. G. K. Maki and J. H. Tracey. A state assignment procedure for asynchronous sequential circuits. *IEEE Transactions on Computers*, 20:666–668, June 1971.

243. G. K. Maki, J. H. Tracey, and R. J. Smith. Generation of design equations in asynchronous sequential circuits. *IEEE Transactions on Computers*, 18:467–472, May 1969.

244. R. Männer. Metastable states in asynchronous digital systems - avoidable or unavoidable. *Microelectronics and Reliability*, 28(2):295–307, 1988.

245. R. Manohar and J. A. Tierno. Asynchronous parallel prefix computation. *IEEE Transactions on Computer-Aided Design*, 47(11):1244–1252, November 1998.

246. L. R. Marino. The effect of asynchronous inputs on sequential network reliability. *IEEE Transactions on Computers*, 26:1082–1090, 1977.

247. L. R. Marino. General theory of metastable operation. *IEEE Transactions on Computers*, C-30(2):107–115, February 1981.

248. A. J. Martin. The probe: An addition to communication primitives. *Information Processing Letters*, 20(3):125–130, 1985. Erratum: *IPL* 21(2):107, 1985.

249. A. J. Martin. Compiling communicating processes into delay-insensitive VLSI circuits. *Distributed Computing*, 1(4):226–234, 1986.

250. A. J. Martin. A synthesis method for self-timed VLSI circuits. In *Proc. International Conference on Computer Design (ICCD)*, pages 224–229, Rye Brook, NY, 1987. IEEE Computer Society Press, Los Alamitos, CA.

251. A. J. Martin. The design of a delay-insensitive microprocessor: An example of circuit synthesis by program transformation. In M. Leeser and G. Brown, editors, *Hardware Specification, Verification and Synthesis: Mathematical Aspects*, volume 408 of *Lecture Notes in Computer Science*, pages 244–259. Springer-Verlag, New York, 1989.

252. A. J. Martin. Formal program transformations for VLSI circuit synthesis. In E. W. Dijkstra, editor, *Formal Development of Programs and Proofs*, UT Year of Programming Series, pages 59–80. Addison-Wesley, Reading, MA, 1989.

253. A. J. Martin. The limitations to delay-insensitivity in asynchronous circuits. In W. J. Dally, editor, *Advanced Research in VLSI*, pages 263–278. MIT Press, Cambridge, MA, 1990.

254. A. J. Martin. Programming in VLSI: From communicating processes to delay-insensitive circuits. In C. A. R. Hoare, editor, *Developments in Concurrency and Communication*, UT Year of Programming Series, pages 1–64. Addison-Wesley, Reading, MA, 1990.

255. A. J. Martin. Synthesis of asynchronous VLSI circuits. In J. Straunstrup, editor, *Formal Methods for VLSI Design*, chapter 6, pages 237–283. North-Holland, Amsterdam, 1990.

256. A. J. Martin. Asynchronous datapaths and the design of an asynchronous adder. *Formal Methods in System Design*, 1(1):119–137, July 1992.

257. A. J. Martin, S. M. Burns, T. K. Lee, D. Borkovic, and P. J. Hazewindus. The design of an asynchronous microprocessor. In C. L. Seitz, editor, *Advanced Research in VLSI*, pages 351–373. MIT Press, Cambridge, MA, 1989.

258. A. J. Martin, S. M. Burns, T. K. Lee, D. Borkovic, and P. J. Hazewindus. The first asynchronous microprocessor: The test results. *Computer Architecture News*, 17(4):95–110, June 1989.

259. A. J. Martin, A. Lines, R. Manohar, M. Nystroem, P. Penzes, R. Southworth, and U. Cummings. The design of an asynchronous MIPS R3000 microprocessor. In *Advanced Research in VLSI*, pages 164–181. IEEE Computer Society Press, Los Alamitos, CA, September 1997.

260. A. J. McAuley. Dynamic asynchronous logic for high-speed CMOS systems. *IEEE Journal of Solid-State Circuits*, 27(3):382–388, March 1992.

261. E. J. McCluskey. Minimization of boolean functions. *Bell System Technical Journal*, 35:1417–1444, November 1956.

262. E. J. McCluskey. Fundamental mode and pulse mode sequential circuits. In *Proc. IFIP Congress 1962, Munich, Germany, Information Processing*, pages 725–730. Holland Publishing Co., 1962.

263. E. J. McCluskey. Transient behavior of combinational logic networks. *Redundancy Techniques for Computing Systems*, pages 9–46, 1962.

264. K. McMillan. Using unfoldings to avoid the state explosion problem in the verification of asynchronous circuits. In G. v. Bochman and D. K. Probst, editors, *Proc. International Workshop on Computer Aided Verification*, volume 663 of *Lecture Notes in Computer Science*, pages 164–177. Springer-Verlag, New York, 1992.

265. K. McMillan and D. L. Dill. Algorithms for interface timing verification. In *Proc. International Conference on Computer Design (ICCD)*. IEEE Computer Society Press, Los Alamitos, CA, 1992.

266. K. L. McMillan. Trace theoretic verification of asynchronous circuits using unfoldings. In *Proc. International Workshop on Computer Aided Verification*, 1995.

267. T. H.-Y. Meng. *Synchronization Design for Digital Systems*. Kluwer Academic Publishers, Boston, 1991. Contributions by D. Messerschmitt, S. Nowick, and D. Dill.

268. T. H.-Y. Meng, R. W. Brodersen, and D. G. Messerschmitt. Automatic synthesis of asynchronous circuits from high-level specifications. *IEEE Transactions on Computer-Aided Design*, 8(11):1185–1205, November 1989.

269. T. H.-Y. Meng, R. W. Brodersen, and D. G. Messerschmitt. Asynchronous design for programmable digital signal processors. *IEEE Transactions on Signal Processing*, 39(4):939–952, April 1991.

270. E. Mercer and C. J. Myers. Stochastic cycle period analysis in timed circuits. In *Proc. International Symposium on Circuits and Systems*, May 2000.

271. G. De Micheli. *Synthesis and Optimization of Digital Circuits*. McGraw-Hill, New York, 1994.

272. R. E. Miller. *Sequential Circuits and Machines*, volume 2 of *Switching Theory*. Wiley, New York, 1965.

273. D. Misunas. Petri nets and speed independent design. *Communications of the ACM*, 16(8):474–481, August 1973.

274. C. E. Molnar, T.-P. Fang, and F. U. Rosenberger. Synthesis of delay-insensitive modules. In H. Fuchs, editor, *Proc. 1985 Chapel Hill Conference on Very Large Scale Integration*, pages 67–86. Computer Science Press, Rockville, MD, 1985.

275. C. E. Molnar, I. W. Jones, W. S. Coates, J. K. Lexau, S. M. Fairbanks, and I. E. Sutherland. Two FIFO ring performance experiments. *Proceedings of the IEEE*, 87(2):297–307, February 1999.

276. Y. Mukai and Y. Tohma. A method for the realization of fail-safe asynchronous sequential circuits. *IEEE Transactions on Computers*, 23(7):736–739, July 1974.

277. D. E. Muller. Asynchronous logics and application to information processing. In *Proc. Symposium on the Application of Switching Theory to Space Technology*, pages 289–297, Stanford, CA, 1962. Stanford University Press.

278. D. E. Muller. The general synthesis problem for asynchronous digital networks. In *Annual Symposium on Switching and Automata Theory*, New York, 1967.

279. D. E. Muller and W. S. Bartky. A theory of asynchronous circuits. In *Proc. International Symposium on the Theory of Switching*, pages 204–243, Cambridge, MA, April 1959. Harvard University Press.

280. T. Murata. Petri nets: Properties, analysis, applications. *Proceedings of the IEEE*, 77(4):541–580, April 1989.

281. C. Myers and H. Jacobson. Efficient exact two-level hazard-free logic minimization. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, March 2001.

282. C. Myers and T. H.-Y. Meng. Synthesis of timed asynchronous circuits. In *Proc. International Conference on Computer Design (ICCD)*, pages 279–282. IEEE Computer Society Press, Los Alamitos, CA, October 1992.

283. C. J. Myers. *Computer-Aided Synthesis and Verification of Gate-Level Timed Circuits*. PhD thesis, Stanford University, October 1995.

284. C. J. Myers, P. A. Beerel, and T. H.-Y. Meng. Technology mapping of timed circuits. In *Asynchronous Design Methodologies*, IFIP Transactions, pages 138–147. Elsevier Science Publishers, New York, May 1995.

285. C. J. Myers and T. H.-Y. Meng. Synthesis of timed asynchronous circuits. *IEEE Transactions on VLSI Systems*, 1(2):106–119, June 1993.

286. C. J. Myers, T. G. Rokicki, and T. H.-Y. Meng. Automatic synthesis of gate-level timed circuits with choice. In *Advanced Research in VLSI*, pages 42–58. IEEE Computer Society Press, Los Alamitos, CA, 1995.

287. C. J. Myers, T. G. Rokicki, and T. H.-Y. Meng. POSET timing and its application to the synthesis and verification of gate-level timed circuits. *IEEE Transactions on Computer-Aided Design*, 18(6):769–786, June 1999.

288. T. Nanya, A. Takamura, M. Kuwako, M. Imai, T. Fujii, M. Ozawa, I. Fukasaku, Y. Ueno, F. Okamoto, H. Fujimoto, O. Fujita, M. Yamashina, and M. Fukuma. TITAC-2: A 32-bit scalable-delay-insensitive microprocessor. In *Symposium Record of HOT Chips IX*, pages 19–32, August 1997.

289. T. Nanya and Y. Tohma. On universal single transition time asynchronous state assignments. *IEEE Transactions on Computers*, 27(8):781–782, August 1978.

290. T. Nanya and Y. Tohma. Universal multicode STT state assignments for asynchronous sequential machines. *IEEE Transactions on Computers*, 28(11):811–818, November 1979.

291. T. Nanya, Y. Ueno, H. Kagotani, M. Kuwako, and A. Takamura. TITAC: Design of a quasi-delay-insensitive microprocessor. *IEEE Design and Test of Computers*, 11(2):50–63, 1994.

292. R. Negulescu and A. Peeters. Verification of speed-dependences in single-rail handshake circuits. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 159–170, 1998.

293. C. D. Nielsen and A. J. Martin. Design of a delay-insensitive multiply-accumulate unit. *Integration, the VLSI Journal*, 15(3):291–311, October 1993.

294. L. S. Nielsen, C. Niessen, J. Sparsø, and C. H. van Berkel. Low-power operation using self-timed and adaptive scaling of the supply voltage. *IEEE Transactions on VLSI Systems*, 2(4):391–397, December 1994.

295. L. S. Nielsen and J. Sparsø. Designing asynchronous circuits for low-power: An IFIR filter bank for a digital hearing aid. *Proceedings of the IEEE*, 87(2):268–281, February 1999.

296. B. J. Nordmann. Modular asynchronous control design. *IEEE Transactions on Computers*, 26(3):196–207, March 1977.

297. S. M. Nowick. Design of a low-latency asynchronous adder using speculative completion. *IEE Proceedings, Computers and Digital Techniques*, 143(5):301–307, September 1996.

298. S. M. Nowick and D. L. Dill. Exact two-level minimization of hazard-free logic with multiple-input changes. *IEEE Transactions on Computer-Aided Design*, 14(8):986–997, August 1995.

299. S. M. Nowick, N. K. Jha, and F.-C. Cheng. Synthesis of asynchronous circuits for stuck-at and robust path delay fault testability. *IEEE Transactions on Computer-Aided Design*, 16(12):1514–1521, December 1997.

300. S. M. Nowick, K. Y. Yun, and P. A. Beerel. Speculative completion for the design of high-performance asynchronous dynamic adders. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 210–223. IEEE Computer Society Press, Los Alamitos, CA, April 1997.

301. S.M. Nowick. *Automatic Synthesis of Burst-Mode Asynchronous Controllers.* PhD thesis, March 1993.

302. S. M. Ornstein, M. J. Stucki, and W. A. Clark. A functional description of macromodules. In *AFIPS Conference Proc.: 1967 Spring Joint Computer Conference*, volume 30, pages 337–355. Academic Press, New York, 1967.

303. J. S. Ostroff. *Temporal Logic for Real-Time Systems.* Wiley, New York, Taunton, England, 1989.

304. H. Özdemir, A. Kepkep, B. Pamir, Y. Leblebici, and U. Çilingiroğlu. A capacitive threshold-logic gate. *IEEE Journal of Solid-State Circuits*, 31(8):1141–1150, August 1996.

305. E. Pastor, J. Cortadella, A. Kondratyev, and O. Roig. Structural methods for the synthesis of speed-independent circuits. *IEEE Transactions on Computer-Aided Design*, 17(11):1108–1129, November 1998.

306. M. C. Paull and S. H. Unger. Minimizing the number of states in incompletely specified sequential switching functions. *IRE Transactions on Electronic Computers*, EC-8:356–367, September 1959.

307. R. C. Pearce, J. A. Field, and W. D. Little. Asynchronous arbiter module. *IEEE Transactions on Computers*, 24:931–932, September 1975.

308. M. Pechoucek. Anomalous response times of input synchronizers. *IEEE Transactions on Computers*, 25(2):133–139, February 1976.

309. A. Peeters. The "Asynchronous" Bibliography (BIBTEX) database file `async.bib`. `http://www.win.tue.nl/cs/pa/wsinap/doc/async.bib`. Corresponding e-mail address: `async-bib@win.tue.nl`.

310. M. A. Peña, J. Cortadella, A. Kondratyev, and E. Pastor. Formal verification of safety properties in timed circuits. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 2–11. IEEE Computer Society Press, Los Alamitos, CA, April 2000.

311. J. L. Peterson. *Petri Net Theory and the Modeling of Systems.* Prentice Hall, 1981.

312. C. A. Petri. Communication with automata. Technical Report RADC-TR-65-377, Vol. 1, Suppl. 1, Applied Data Research, Princeton, NJ, 1966.

313. C. Piguet. Logic synthesis of race-free asynchronous CMOS circuits. *IEEE Journal of Solid-State Circuits*, 26(3):371–380, March 1991.

314. M. Pipponzi and F. Somenzi. An iterative approach to the binate covering problem. In *Proc. European Conference on Design Automation (EDAC)*, pages 208–211, March 1990.

315. W. W. Plummer. Asynchronous arbiters. *IEEE Transactions on Computers*, 21(1):37–42, January 1972.

316. A. Pnueli. The temporal logic of programs. In *Proc. 18th IEEE Symposium on Foundations of Computer Science*, pages 46–57, 1977.

317. D. K. Probst and H. F. Li. Using partial-order semantics to avoid the state explosion problem in asynchronous systems. In R. P. Kurshan and E. M. Clarke, editors, *Proc. International Workshop on Computer Aided Verification*, volume 531 of *Lecture Notes in Computer Science*, pages 146–155. Springer-Verlag, New York, 1990.

318. G. R. Putzolu. A heuristic algorithm for the testing of asynchronous circuits. *IEEE Transactions on Computers*, 20(6):639–647, June 1970.

319. R. Ramachandran and S.-L. Lu. Efficient arithmetic using self-timing. *IEEE Transactions on VLSI Systems*, 4(4):445–454, December 1996.

320. C. Ramchandani. Analysis of asynchronous concurrent systems by timed Petri nets. Technical Report 120, Project MAC, MIT, Cambridge, MA, February 1974.

321. M. Renaudin, B. El Hassan, and A. Guyot. New asynchronous pipeline scheme: Application to the design of a self-timed ring divider. *IEEE Journal of Solid-State Circuits*, 31(7):1001–1013, July 1996.

322. C. A. Rey and J. Vaucher. Self-synchronized asynchronous sequential machines. *IEEE Transactions on Computers*, 23(12):1306–1311, December 1974.

323. J. Rho, G. Hachtel, F. Somenzi, and R. Jacoby. Exact and heuristic algorithms for the minimization of incompletely specified state machines. *IEEE Transactions on Computer-Aided Design*, pages 167–177, February 1994.

324. W. F. Richardson and E. Brunvand. Architectural considerations for a self-timed decoupled processor. *IEE Proceedings, Computers and Digital Techniques*, 143(5):251–257, September 1996.

325. T. G. Rokicki. *Representing and Modeling Circuits.* PhD thesis, Stanford University, 1993.

326. T. G. Rokicki and C. J. Myers. Automatic verificaton of timed circuits. In *Proc. International Conference on Computer Aided Verification*, pages 468–480. Springer-Verlag, New York, 1994.

327. F. U. Rosenberger and C. E. Molnar. Comments on "metastability of CMOS latch/flip-flop". *IEEE Journal of Solid-State Circuits*, 27(1):128–130, January 1992. Reply by Robert W. Dutton, pages 131–132 of same issue.

328. F. U. Rosenberger, C. E. Molnar, T. J. Chaney, and T.-P. Fang. Q-modules: Internally clocked delay-insensitive modules. *IEEE Transactions on Computers*, C-37(9):1005–1018, September 1988.

329. L. Y. Rosenblum and A. V. Yakovlev. Signal graphs: From self-timed to timed ones. In *Proc. of International Workshop on Timed Petri Nets*, pages 199–207, Torino, Italy, July 1985. IEEE Computer Society Press, Los Alamitos, CA.

330. S. Rotem, K. Stevens, R. Ginosar, P. Beerel, C. Myers, K. Yun, R. Kol, C. Dike, M. Roncken, and B. Agapiev. RAPPID: An asynchronous instruction length decoder. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 60–70, April 1999.

331. G. A. Ruiz. Evaluation of three 32-bit CMOS adders in DCVS logic for self-timed circuits. *IEEE Journal of Solid-State Circuits*, 33(4):604–613, April 1998.

332. J. Rutten and M. Berkelaar. Efficient exact and heuristic minimization of hazard-free logic. In *Proc. International Conference on Computer Design (ICCD)*, pages 152–159, October 1998.

333. J. W. J. M. Rutten and M. R. C. M. Berkelaar. Improved state assignments for burst mode finite state machines. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 228–239. IEEE Computer Society Press, Los Alamitos, CA, April 1997.

334. J. W. J. M. Rutten, M. R. C. M. Berkelaar, C. A. J. van Eijk, and M. A. J. Kolsteren. An efficient divide and conquer algorithm for exact hazard free logic minimization. In *Proc. Design, Automation and Test in Europe (DATE)*, pages 749–754, April 1998.

335. T. Sakurai. Optimization of CMOS arbiter and synchronizer circuits with submicron MOSFETs. *IEEE Journal of Solid-State Circuits*, 23(4):901–906, August 1988.

336. M. Santoro and M. A. Horowitz. SPIM: A pipelined 64 × 64-bit iterative multiplier. *IEEE Journal of Solid-State Circuits*, 24(2):487–493, April 1989.

337. G. Saucier. Encoding of asynchronous sequential networks. *IEEE Transactions on Electronic Computers*, EC-16:365–369, June 1967.

338. G. Saucier. State assignment of asynchronous sequential machines using graph techniques. *IEEE Transactions on Computers*, 21:282–288, March 1972.

339. M. H. Sawasaki, C. Ykman-Couvreur, and B. Lin. Externally hazard-free implementations of asynchronous control circuits. *IEEE Transactions on Computer-Aided Design*, 16(8):835–848, August 1997.

340. D. H. Sawin and G. K. Maki. Asynchronous sequential machines designed for fault detection. *IEEE Transactions on Computers*, C-23(3):239–249, March 1974.

341. S. Schuster, W. Reohr, P. Cook, D. Heidel, M. Immediato, and K. Jenkins. Asynchronous interlocked pipelined CMOS circuits operating at 3.3-4.5 GHz. In *Proc. International Solid State Circuits Conference*, February 2000.

342. C-J. Seger and J.A. Brzozowski. An optimistic ternary simulation of gate races. *Theoretical Computer Science*, 61(1):49–66, October 1988.

343. C. Seitz. *Graph Representations for Logical Machines.* PhD thesis, Massachusetts Institute of Technology, 1971.

344. C. L. Seitz. Asynchronous machines exhibiting concurrency, 1970. *Record of the Project MAC Concurrent Parallel Computation.*

345. C. L. Seitz. Self-timed VLSI systems. In C. L. Seitz, editor, *Proc. First Caltech Conference on Very Large Scale Integration*, pages 345–355, Pasadena, CA, January 1979.

346. C. L. Seitz. Ideas about arbiters. *Lambda*, 1(1, First Quarter):10–14, 1980.

347. C. L. Seitz. System timing. In C. A. Mead and L. A. Conway, editors, *Introduction to VLSI Systems*, chapter 7. Addison-Wesley, Reading, MA, 1980.

348. J. N. Seizovic. Pipeline synchronization. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 87–96, November 1994.

349. A. Semenov and A. Yakovlev. Verification of asynchronous circuits using time Petri-net unfolding. In *Proc. ACM/IEEE Design Automation Conference*, pages 59–63, 1996.

350. A. Semenov, A. Yakovlev, E. Pastor, M. Peña, and J. Cortadella. Synthesis of speed-independent circuits from STG-unfolding segment. In *Proc. ACM/IEEE Design Automation Conference*, pages 16–21, 1997.

351. P. Siegel and G. De Micheli. Decomposition methods for library binding of speed-independent asynchronous designs. In *Proc. International Conference on Computer-Aided Design (ICCAD)*, pages 558–565, November 1994.

352. P. Siegel, G. De Micheli, and D. Dill. Automatic technology mapping for generalized fundamental-mode asynchronous designs. In *Proc. ACM/IEEE Design Automation Conference*, pages 61–67, June 1993.

353. P. S. K. Siegel. *Automatic Technology Mapping for Asynchronous Designs.* PhD thesis, Stanford University, February 1995.

354. M. Singh and S. M. Nowick. High-throughput asynchronous pipelines for fine-grain dynamic datapaths. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 198–209. IEEE Computer Society Press, Los Alamitos, CA, April 2000.

355. V. W.-Y. Sit, C.-S. Choy, and C.-F. Chan. Use of current sensing technique in designing asynchronous static RAM for self-timed systems. *Electronics Letters*, 33(8):667–668, 1997.

356. V. W.-Y. Sit, C.-S. Choy, and C.-F. Chan. A four-phase handshaking asynchronous static RAM design for self-timed systems. *IEEE Journal of Solid-State Circuits*, 34(1):90–96, January 1999.

357. A. E. Sjogren and C. J. Myers. Interfacing synchronous and asynchronous modules within a high-speed pipeline. 8(5):573–583, October 2000.

358. J. R. Smith and C. H. Roth. Analysis and synthesis of asynchronous sequential network using edge-sensitive flip-flops. *IEEE Transactions on Computers*, 20:847–855, 1971.

359. R. J. Smith. Generation of internal state assignments for large asynchronous sequential machines. *IEEE Transactions on Computers*, 23:924–932, September 1974.

360. J. Snepscheut. Deriving circuits from programs. In R. Bryant, editor, *Proc. 3rd Caltech Conference on VLSI*, pages 241–256. Computer Science Press, Rockville, MD, 1983.

361. J. L. A. van de Snepscheut. *Trace Theory and VLSI Design*, volume 200 of *Lecture Notes in Computer Science.* Springer-Verlag, New York, 1985.

362. R. F. Sproull and I. E. Sutherland. Stoppable clock. *Technical Memo 3438*, Sutherland, Sproull, and Associates, January, 1985.

363. R. F. Sproull and I. E. Sutherland. *Asynchronous Systems*. Sutherland, Sproull, and Associates, Palo Alto, CA, 1986. Vol. I: *Introduction*, Vol. II: *Logical Effort and Asynchronous Modules*, Vol. III: *Case Studies*.

364. R. F. Sproull, I. E. Sutherland, and C. E. Molnar. The counterflow pipeline processor architecture. *IEEE Design and Test of Computers*, 11(3):48–59, Fall 1994.

365. K. Stevens. Private communication, September 2000. Ken Stevens is with Intel Corporation.

366. K. Stevens, R. Ginosar, and S. Rotem. Relative timing. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 208–218, April 1999.

367. K. Stevens, S. Rotem, R. Ginosar, P. Beerel, C. Myers, K. Yun, R. Kol, C. Dike, and M. Roncken. An asynchronous instruction length decoder. *IEEE Journal of Solid-State Circuits*, 35(2):217–228, February 2001.

368. M. J. Stucki and J. R. Cox. Synchronization strategies. In C. L. Seitz, editor, *Proc. First Caltech Conference on Very Large Scale Integration*, pages 375–393, 1979.

369. M. J. Stucki, S. M. Ornstein, and W. A. Clark. Logical design of macromodules. In *AFIPS Conference Proc.: 1967 Spring Joint Computer Conference*, volume 30, pages 357–364. Academic Press, New York, 1967.

370. I. E. Sutherland. Micropipelines. *Communications of the ACM*, 32(6):720–738, June 1989.

371. I. E. Sutherland, C. E. Molnar, R. F. Sproull, and J. C. Mudge. The trimosbus. In C. L. Seitz, editor, *Proc. of the First Caltech Conference on Very Large Scale Integration*, pages 395–427, 1979.

372. Ivan Sutherland and Scott Fairbanks. GasP: A minimal FIFO control. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 46–53. IEEE Computer Society Press, Los Alamitos, CA, March 2001.

373. H. Takata, S. Komori, T. Tamura, F. Asai, H. Satoh, T. Ohno, T. Tokuda, H. Nishikawa, and H. Terada. A 100-mega-access per second matching memory for a data-driven microprocessor. *IEEE Journal of Solid-State Circuits*, 25(1):95–99, February 1990.

374. C. J. Tan. State assignments for asynchronous sequential machines. *IEEE Transactions on Computers*, 20(4):382–391, April 1971.

375. G. S. Taylor and G. M. Blair. Reduced complexity two-phase micropipeline latch controller. *IEEE Journal of Solid-State Circuits*, 33(10):1590–1593, October 1998.

376. H. Terada, S. Miyata, and M. Iwata. DDMP's: Self-timed super-pipelined data-driven multimedia processors. *Proceedings of the IEEE*, 87(2):282–296, February 1999.

377. R. A. Thacker, W. Belluomini, and C. J. Myers. Timed circuit synthesis using implicit methods. In *Proc. International Conference on VLSI Design*, pages 181–188, 1999.

378. M. Theobald and S. M. Nowick. Fast heuristic and exact algorithms for two-level hazard-free logic minimization. *IEEE Transactions on Computer-Aided Design*, 17(11):1130–1147, November 1998.

379. J. A. Tierno, A. J. Martin, D. Borkovic, and T. K. Lee. A 100-MIPS GaAs asynchronous microprocessor. *IEEE Design and Test of Computers*, 11(2):43–49, 1994.

380. J. H. Tracey. Internal state assignments for asynchronous sequential machines. *IEEE Transactions on Electronic Computers*, EC-15:551–560, August 1966.

381. J. T. Udding. A formal model for defining and classifying delay-insensitive circuits. *Distributed Computing*, 1(4):197–204, 1986.

382. S. H. Unger. *Asynchronous Sequential Switching Circuits*. Wiley-Interscience, New York, 1969.

383. S. H. Unger. Asynchronous sequential switching circuits with unrestricted input changes. *IEEE Transactions on Computers*, 20(12):1437–1444, December 1971.

384. S. H. Unger. Self-synchronizing circuits and nonfundamental mode operation. *IEEE Transactions on Computers*, 26(3):278–281, March 1977.

385. S. H. Unger. Hazards, critical races, and metastability. *IEEE Transactions on Computers*, 44(6):754–768, June 1995.

386. V. Vakilotojar and P. A. Beerel. RTL verification of asynchronous and heterogeneous systems using symbolic model checking. *Integration, the VLSI Journal*, 24(1):19–36, December 1997.

387. M. Valencia, M. J. Bellido, J. L. Huertas, A. J. Acosta, and S. Sanchez-Solano. Modular asynchronous arbiter insensitive to metastability. *IEEE Transactions on Computers*, 44(12):1456–1461, December 1995.

388. A. Valmari. A stubborn attack on state explosion. In *Proc. International Workshop on Computer Aided Verification*, pages 176–185, June 1990.

389. P. Vanbekbergen. *Synthesis of Asynchronous Control Circuits from Graph-Theoretic Specifications*. PhD thesis, Catholic University of Leuven, September 1993.

390. P. Vanbekbergen, G. Goossens, F. Catthoor, and H. J. de Man. Optimized synthesis of asynchronous control circuits from graph-theoretic specifications. *IEEE Transactions on Computer-Aided Design*, 11(11):1426–1438, November 1992.

391. P. Vanbekbergen, B. Lin, G. Goossens, and H. de Man. A generalized state assignment theory for transformations on signal transition graphs. *Journal of VLSI Signal Processing*, 7(1/2):101–115, February 1994.

392. W. S. VanScheik and R. F. Tinder. High speed externally asynchronous / internally clocked systems. *IEEE Transactions on Computers*, 46(7):824–829, July 1997.

393. V. I. Varshavsky, editor. *Self-Timed Control of Concurrent Processes: The Design of Aperiodic Logical Circuits in Computers and Discrete Systems.* Kluwer Academic Publishers, Boston, Dordrecht, The Netherlands, 1990.

394. H. J. M. Veendrick. The behavior of flip-flops used as synchronizers and prediction of their failure rate. *IEEE Journal of Solid-State Circuits*, 15(2):169–176, 1980.

395. P. Vingron. Coherent design of asynchronous circuits. *IEE Proceedings, Computers and Digital Techniques*, 130(6):190–202, 1983.

396. W. M. Waite. The production of completion signals by asynchronous, iterative networks. *IEEE Transactions on Computers*, 13(2):83–86, April 1964.

397. J. Walker and A. Cantoni. A new synchronizer design. *IEEE Transactions on Computers*, 45(11):1308–1311, November 1996.

398. D. T. Weih and M. R. Greenstreet. Verification of speed-independent data-path circuits. *IEE Proceedings, Computers and Digital Techniques*, 143(5):295–300, September 1996.

399. S. R. Whitaker and G. K. Maki. Pass-transistor asynchronous sequential circuits. *IEEE Journal of Solid-State Circuits*, 24(1):71–78, February 1989.

400. T. Williams, N. Patkar, and G. Shen. SPARC64: A 64-b 64-active-instruction out-of-order-execution MCM processor. *IEEE Journal of Solid-State Circuits*, 30(11):1215–1226, November 1995.

401. T. E. Williams. *Self-Timed Rings and Their Application to Division.* PhD thesis, Stanford University, June 1991.

402. T. E. Williams. Performance of iterative computation in self-timed rings. *Journal of VLSI Signal Processing*, 7(1/2):17–31, February 1994.

403. T. E. Williams and M. A. Horowitz. Bipolar circuit elements providing self-completion-indication. *IEEE Journal of Solid-State Circuits*, 25(1):309–312, January 1990.

404. T. E. Williams and M. A. Horowitz. A zero-overhead self-timed 160ns 54b CMOS divider. *IEEE Journal of Solid-State Circuits*, 26(11):1651–1661, November 1991.

405. A. S. Wojcik and K.-Y. Fang. On the design of three-valued asynchronous modules. *IEEE Transactions on Computers*, 29(10):889–898, October 1980.

406. J. V. Woods, P. Day, S. B. Furber, J. D. Garside, N. C. Paver, and S. Temple. AMULET1: An asynchronous ARM processor. *IEEE Transactions on Computers*, 46(4):385–398, April 1997.

407. S.-F. Wu and P. D. Fisher. Automating the design of asynchronous sequential logic circuits. *IEEE Journal of Solid-State Circuits*, 26(3):364–370, March 1991.

408. A. Xie and P. A. Beerel. Performance analysis of asynchronous circuits and systems using stochastic timed Petri nets. In A. Yakovlev, L. Gomes, and L. Lavagno, editors, *Hardware Design and Petri Nets*, pages 239–268. Kluwer Academic Publishers, Boston, March 2000.

409. A. Yakovlev, A. Petrov, and L. Lavagno. A low latency asynchronous arbitration circuit. *IEEE Transactions on VLSI Systems*, 2(3):372–377, September 1994.

410. T. Yamasaki, K. Shima, S. Komori, H. Takata, T. Tamura, F. Asai, T. Ohno, O. Tomisawa, and H. Terada. VLSI implementation of a variable-length pipeline scheme for data-driven processors. *IEEE Journal of Solid-State Circuits*, 24(4):933–937, August 1989.

411. O. Yenersoy. Synthesis of asynchronous machines using mixed-operation mode. *IEEE Transactions on Computers*, 28(4):325–329, 1979.

412. C. Ykman-Couvreur and B. Lin. Efficient state assignment framework for asynchronous state graphs. In *Proc. International Conference on Computer Design (ICCD)*, pages 692–697. IEEE Computer Society Press, Los Alamitos, CA, 1995.

413. C. Ykman-Couvreur and B. Lin. Optimised state assignment for asynchronous circuit synthesis. In *Asynchronous Design Methodologies*, pages 118–127. IEEE Computer Society Press, Los Alamitos, CA, May 1995.

414. T. Yoneda and H. Ryu. Timed trace theoretic verification using partial order reduction. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 108–121, April 1999.

415. T. Yoneda and B. Schlingloff. Efficient verification of parallel real-time systems. In C. Courcoubetis, editor, *Formal Methods in System Design*. Kluwer Academic Publishers, Boston, 1997.

416. T. Yoneda and T. Yoshikawa. Using partial orders for trace theoretic verification of asynchronous circuits. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*. IEEE Computer Society Press, Los Alamitos, CA, March 1996.

417. S. Yovine. KRONOS: A verification tool for real-time systems. *Springer International Journal of Software Tools for Technology Transfer*, 1(1/s2), October 1997.

418. K. Y. Yun. *Synthesis of Asynchronous Controllers for Heterogeneous Systems*. PhD thesis, Stanford University, August 1994.

419. K. Y. Yun, P. A. Beerel, V. Vakilotojar, A. E. Dooply, and J. Arceo. The design and verification of a high-performance low-control-overhead asynchronous differential equation solver. *IEEE Transactions on VLSI Systems*, 6(4):643–655, December 1998.

420. K. Y. Yun and D. L. Dill. Automatic synthesis of extended burst-mode circuits i: Specification and hazard-free implementation. *IEEE Transactions on Computer-Aided Design*, 18(2):101–117, February 1999.

421. K. Y. Yun and D. L. Dill. Automatic synthesis of extended burst-mode circuits II: Automatic synthesis. *IEEE Transactions on Computer-Aided Design*, 18(2):118–132, February 1999.

422. K. Y. Yun, D. L. Dill, and S. M. Nowick. Practical generalizations of asynchronous state machines. In *Proc. European Conference on Design Automation (EDAC)*, pages 525–530. IEEE Computer Society Press, Los Alamitos, CA, February 1993.

423. K. Y. Yun and A. E. Dooply. Pausible clocking-based heterogeneous systems. *IEEE Transactions on VLSI Systems*, 7(4):482–488, December 1999.

424. K. Y. Yun, B. Lin, D. L. Dill, and S. Devadas. BDD-based synthesis of extended burst-mode controllers. *IEEE Transactions on Computer-Aided Design*, 17(9):782–792, September 1998.

425. B. Zhou, T. Yoneda, and B.-G. Schlingloff. Conformance and mirroring for timed asynchronous circuits. In *Proc. Asia and South Pacific Design Automation Conference*, 2001.